A Microreplicated Pad for Tungsten Chemical-Mechanical Planarization

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A microreplicated (MR) pad with regulated long-range order surface pore-asperity patterns is used for the buff polish step in a 3-platen W-CMP process for 14 nm replacement metal gate (RMG) and trench salicide (TS) planarization. This new pad requires no diamond tip conditioner and can last up to 2000 wafer passes with highly repeatable removal rates, while maintaining low and consistent defects and within-wafer uniformity. The MR pad also provides unique benefits of mitigating within-die non-uniformity as demonstrated by gate electrical conductance tests and confirmed by physical thickness measurement through cross-sectional TEM. In addition, topography-driven defects are reduced significantly. The mechanisms responsible for the unique performance of MR pads will be elucidated and the significance of this new CMP pad technology will be discussed.

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Chemical-mechanical planarization (CMP) has become a pivotal manufacturing process for new integration schemes of semiconductor devices ever since its invention in the 1980s. From the implementation of Cu interconnects early on to the realization of field-effect transistors (FinFET) for 22 nm technology and beyond, CMP is *the process* that enables leading-edge device performance. With shrinking feature size for advanced technology nodes, however, the planarity requirements for CMP are tightened down to the order of several nanometers across the entire 300 mm wafer. Meanwhile, the tolerance for non-uniformity reduces to only a few percent *within-die*, *within-wafer*, and *wafer-to-wafer* for 14 nm technology nodes and above. As a consequence, advances in CMP equipment and consumables are urgently need in order to meet such stringent planarity and uniformity criteria.

Conventional approaches to within-wafer CMP planarity and uniformity control such as the optimization of polish pressure, platen/carrier rotation, slurry flow, pad conditioning, slurry components, and so forth have become the standard practice at the end-user level. Coupled with advances in equipment technologies, the above approaches provide wafer to sub-wafer level thickness and planarity correction. When combined with metrology-based advanced process control (APC), they can help reduce *wafer-to-wafer* variation as well. Recent progress in RIE technology also enables across-wafer thickness correction *die by die* and assists CMP to achieve *nano-scale* within-wafer uniformity.[1,2] However, there is still a lack of effective method to mitigate one of the longest lasting major challenges of CMP, the pattern dependency,[3–5] which would give rise to within-die non-uniformity (WIDNU). As illustrated in Fig. 1, pattern dependency arises when the initial difference in pattern density among various structures creates a global step height variation, due to the difference in removal rates before the local patterns are planarized. In the case of tungsten replacement metal gate (W-RMG) CMP, such within-die gate height variation will translate to drift in gate resistance and threshold voltage across different devices, compromising the performance of the functional die. Improvement in CMP planarization efficiency across all different pattern densities and pitches is urgently needed in order to mitigate WIDNU.

In the past, several approaches have been adopted to enhance CMP planarization efficiency for WIDNU reduction. The inclusion of pattern fill structures (i.e., *dummy patterns*)[6] to optimize the overall pattern density proves effective to certain degrees and has become a common practice in the industry. However, the dummy patterns themselves occupy invaluable space within a die and exerts constraints on IC design, especially for high performance server chips with complicated layout. In the case shallow trench isolation (STI) CMP, the addition of a pre-patterning step, such as reverse etch back to remove most of the oxide in the active area was another common process early on.[7] However, it incurs more steps and costs to the process flow. Plus, defects can be a concern. The application of high-selectivity slurries to improve the ability to halt polishing on the stop layer is also a widely accepted approach.[8] Nevertheless, once stop layer is reached, the selectivity difference would still induce varying amount of dishing across various pattern densities on the non-protected wide area.

At a microscopic scale, the events happening in asperity contact along the pad-wafer interface hold the key to CMP uniformity issues. In an ideal scenario, the distribution of abrasive particles, asperity contacts, and the pressures/shear stress in the interface should be uniform enough to the extent that material removal occurs consistently across the single pattern level (a few nm), single device level (100 nm ∼ 1000 nm), functional level (a few mm), die level (a few cm), and finally, wafer level (tens of cm). In the context of CMP pad, the above scenario would require uniformity in the dimension of grooves, asperity height, pore size and its distribution at all scale levels. In fact, recent advance in pad groove engineering has demonstrated improvement in slurry utilization efficiency and debris removal for WIWNU improvement and defect reduction.[9] In addition, novel pad surface texture design with 3-dimensional interconnected unit cells also enables the possibility of more uniform material removal and maintaining consistent surface area as the pad wears,[10] although its potential for planarization efficiency is yet to be tested.

Fixed-abrasive represents a more radical change in CMP pads technology intended for the improvement of WIWNU and WIDNU.[11,12] With abrasive particles embedded in microreplicated resin patterns on top of pad, the slurry-free CMP process with fixed-abrasive pads simplifies the 3-body pad/abrasive/wafer contact down to only 2-body pad/wafer contact with demonstrated superior planarization efficiency and improved WID uniformity over conventional pad/slurry processes. However, advances in slurry formulation has kept up and can deliver similar or better selectivity. Besides, defects, especially scratches can be an issue for fixed abrasive pads.

A more recent and non-traditional CMP technology for WIDNU improvement is the *pad-in-a-bottle* (PIB) approach.[13,14] In this new technology, polyurethane (PU) polishing pad is replaced by a stiff polycarbonate counterface, and polyurethane beads 10–50 μm in diameter are used in conjunction with slurry and slurry particles to achieve planarization. In other words, the large PU pad surface is transformed into a stiff counterface with numerous circular PU beads in the slurry to transmit the down pressure and assist in planarization. Reduction in WIDNU is demonstrated with PIB for oxide CMP. Process simulation suggests planarization efficiency improvement results from the less bending of the stiff counterface in response to wafer surface topography. In addition, the polyurethane beads in PIB are

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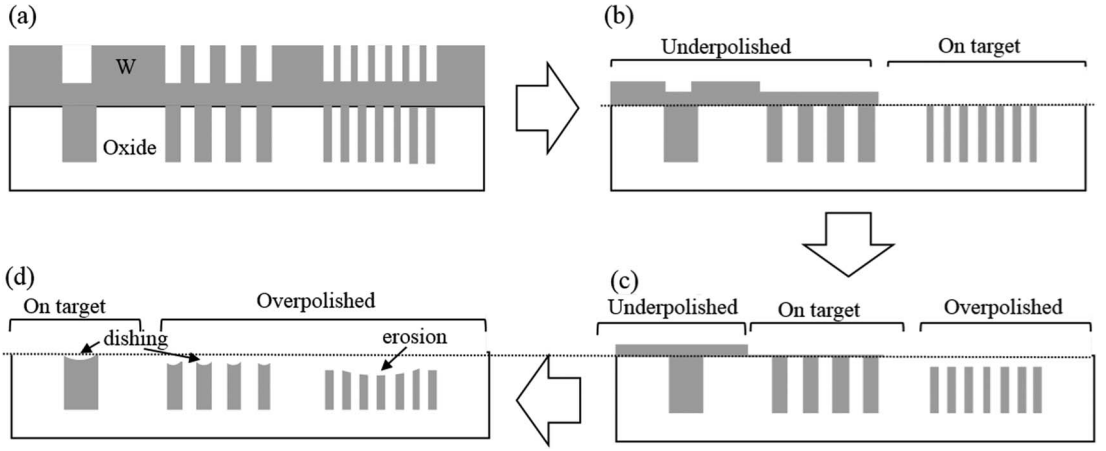

Figure 1. Generation of within-die non-uniformity throughout a W CMP process. (a) Incoming to CMP; (b) partial clear of W overburden; (c) end-point plus certainly amount of overpolish, showing erosion in the array yet still underpolish above large isolated patterns; (d) after oxide buff, thickness and local topography (i.e., dishing and erosion) varations across different pattern densities.

effective at transmitting applied force between slurry abrasives and the wafer surface. However, the PIB approach is still in its development stage and yet to be tested in semiconductor fab environment.

In the present study, a new CMP pad fabricated with advanced *microreplication* (MR) technology is tested for process repeatability and uniformity improvement for tungsten CMP. Previously, MR technology has been applied to produce pad conditioners (*microreplicated conditioners*) with improvements in process stability and defect reduction in high-volume manufacturing (HVM) environment.[15,16] The highly ordered and repeatable tips and patterns on the microreplicated conditioners are thought to have contributed to the more uniform and effective rejuvenation of pad surface asperities, leading to long term rate stability and defect reduction.[16] Carrying the similar concept one step forward, the MR process is now applied to fabricate highly regulated 3-dimensional patterns directly onto pad surface with long range repeatability. It will be demonstrated that such MR pads with specially designed surface patterns give rise to long term removal rate stability without the need for conventional pad dressing with diamond tip conditioner. In addition, the highly regulated surface patterns ensures more uniform material removal across different pitches and pattern densities, resulting in reduction in WIDNU.

Experimental

Microreplicated (MR) CMP pads.—The microreplicated process represents a radical paradigm shift from conventional CMP pad design and manufacturing. The pictures in Fig. 2 illustrate the sharp contrast between conventional and microreplicated pads in their surface features. The MR CMP pad from 3M Company uses precisely engineered three-dimensional microreplicated asperities and pores on polyurethane, ensuring uniform height, diameter, and depth. As depicted in Fig. 3, the pores and asperities are arranged into unit cells for independent movement for uniform pressure across the wafer. An innovative groove design separates each of the unit cells for efficient slurry flow independent from wafer location. The precisely controlled microreplicated asperities and pores ensure consistent performance

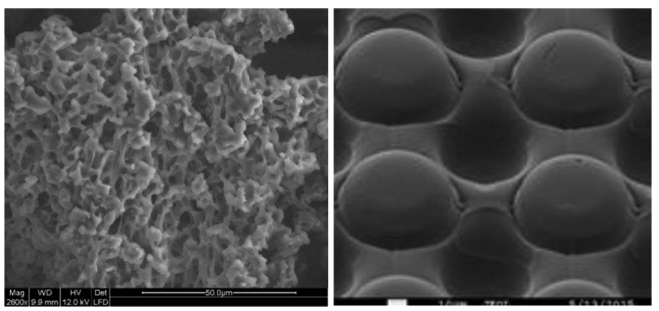

Figure 2. Top view of conventional pad (*left*) and microreplicated pad (*right*). Field of view is 100 μm by 100 μm for both.

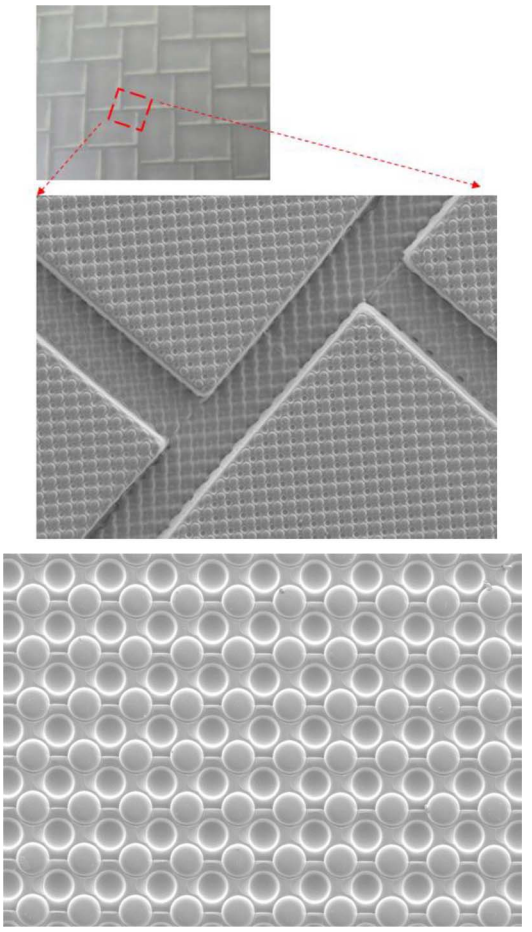

Figure 3. Surface of the microreplicated pad used in the present study: (*top*) 35X magnified view showing unit cells laid out in "Herringbone" pattern with grooves around; (*bottom*) 100X magnified view showing the repeating microreplicated asperities and pores within unit cells.

Table I. Characteristics of the microreplicated pad in the present study.

Pad Characteristics	Target	Unit
Hardness	92	Shore A
Asperity Height	18	μm
Groove Depth	250	μm
Groove Width	450	μm
Total Pad Thickness	118	mil

from run-to-run and pad-to-pad to meet the demands of advanced node CMP processes. The hardness and geometric dimension of the MR pad used in the present study is shown in Table I. For comparison, the process-of-record (POR) W-CMP uses a conventional pad of the same hardness but with concentric grooves.

CMP consumables and process set-up.—All CMP experiments are conducted on 300 mm polisher with 3 platens and a serial cleaning module. Platen 1 is intended for bulk W removal while platen 2 is the W end-pointed step with certain percentage of overpolish to clear W residues. Platen 3 (P3) is liner polish and oxide dielectric trimming polish step. The regular process flow of RMG W CMP consists of 2 steps. Pass 1 CMP removes bulk W and liner, and trims down the dielectric to a pre-determined thicker target. The total RMG gate height is then measured by scatterometry and the data is fed forward to run the P3-only touch-up step, which drives to the final target gate height through APC.

For process-of-record (POR) W-CMP, all wafers were polished with the same consumable set including slurries, pad, conditioners, clean chemicals, and roller brushes unless stated otherwise. Specifically, slurries for both P2 and P3 steps are acidic, silica-based with ferric nitrates and a few percentage of H_2O_2. P2 process shows high W to oxide selectivity while the opposite is true for P3's. The P3 process is a timed polish on a conventional pad with concentric grooves. The P3 pad goes through a 30-min break-in process at the beginning. Ex-situ conditioning is performed for every wafer run with a diamond disk conditioner under a 6lb down force.

The MR-pad CMP process shares exactly the same consumables and process flow as POR, except a MR pad as shown in Fig. 3 is installed on platen 3 for the buff step. In addition, diamond pad conditioner is replaced by a disk of bristle pad cleaning brush. After installing the MR pad, a 15-min pad surface *cleaning* under 2lb down force is performed with the pad brush in lieu of the conventional *pad break-in* process. In-situ pad *cleaning* is also conducted with the brush during each wafer run. In other words, there is no pad cutting by diamond tips in the MR pad CMP process. Pad wear is the direct consequence of the contact with bristle brush and wafer surface.

Wafers.—300 mm W blanket wafers prepared by chemical vapor deposition are chosen to run 2000 W marathon tests. Oxide, TiN_x liner, and W are deposited sequentially onto bare Si wafers to the same thickness as on the integrated 14 nm RMG wafers. These blanket wafers also run through the same full sequence 3-platen CMP processes. 80-point spectroscopic ellipsometer measurements with 3-mm edge exclusion are performed across wafer diameter in order to collect oxide removal and WiWNU data. Surfscan SP3 wafer inspection with 60 nm resolution is conducted and net adders are extracted to monitor the defects throughout 2000 wafer runs.

Integrated patterned wafers for CMP experiments are all silicon-on-insulator (SOI) based fin field effect transistors (FinFET) with deep trench (DT) capacitors, based on 14 nm design ground rule. For RMG W-CMP, high-k dielectric and work function metal (WFM) are deposited on top of the FIN channel. TiN_x liner and tungsten electrode materials are then deposited into the recessed WFM, and polished back by CMP to a gate height target by APC control. For trench salicide (TS) W-CMP, TiN_x liner and tungsten metal are filled into trench and then polished back to provide the local interconnects.

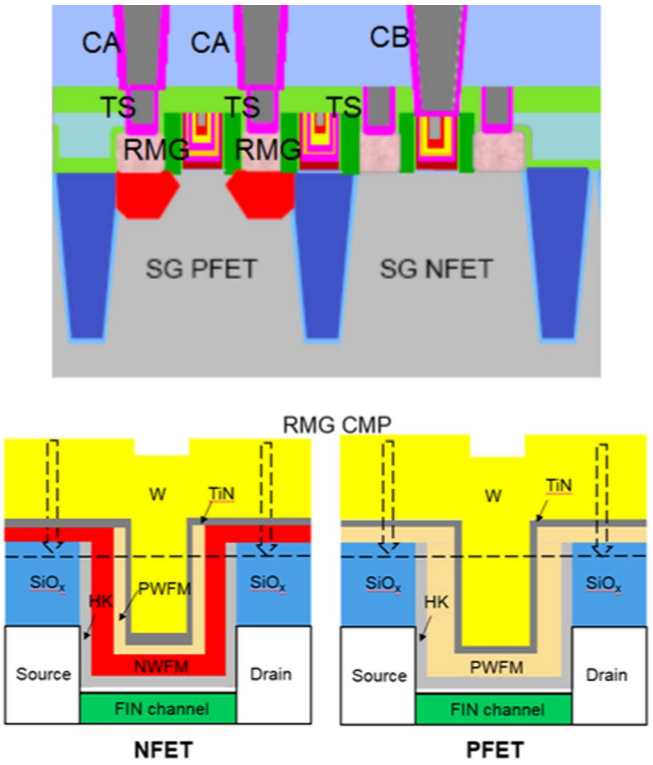

Figure 4. (a) (*Top*) cross-sectional view of a device showing RMG, TS, and CA/CB (i.e., W via contacts) where W-CMP is the enabling process; (b) (*bottom*) schematic of RMG CMP.

The schematic views of tungsten RMG and TS are shown in Fig. 4. Integrated wafers polished with POR process for RMG CMP continue on to receive POR process for TS CMP. The same is true for wafers processed with MR pads.

Results and Discussion

2000 W marathon tests.—Mean oxide removal and its WIWNU is monitored throughout the 2000 W marathon tests. The results are shown in Fig. 5 and Fig. 6. For the POR process, oxide removal shows large variation with an overall increasing trend up to ~1300 W. On the contrary, MR pad exhibits consistent oxide removal with much less variation with increasing wafer counts, despite a slight decrease in rates beyond 1700 W. As depicted in Fig. 6, MR pad also results in lower and more consistent normalized StdDev (1σ) than POR throughout the marathon test.

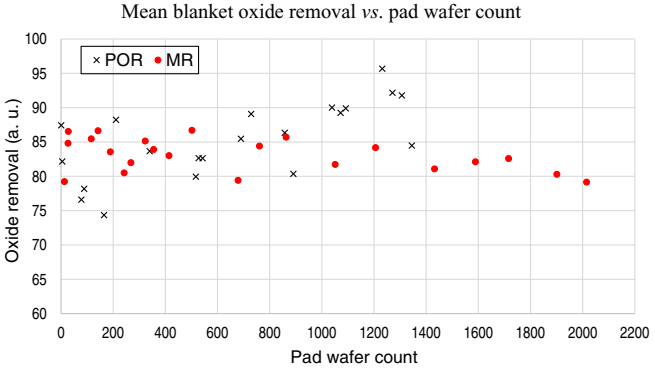

Figure 5. Mean blanket oxide removal vs. pad wafer count for POR and MR pads.

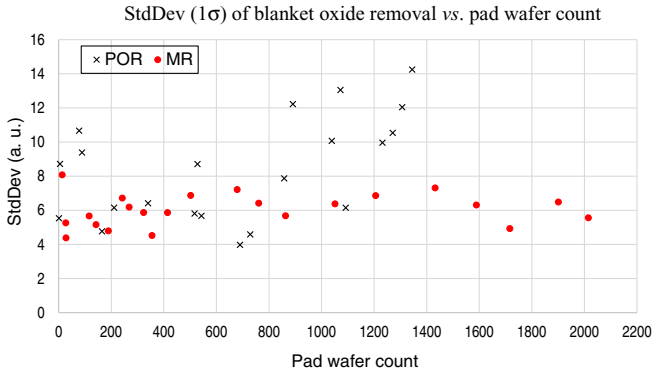

Figure 6. Normalized standard deviation (1σ) of blanket oxide removal vs. pad wafer count for POR and MR pads.

The variation of net defect adders with pad wafer counts from marathon tests is shown in Fig. 7. Once again, it is quite clear that, compared with POR, MR pad leads to low and more consistent defect adders throughout the marathon. There is no discernable difference in the type of defects between the two pads. The majority of them are chatter marks as shown in the picture.

Within-die non-uniformity (WIDNU) and defects improvement.—WIDNU is determined both electrically and physically on fully integrated 14 nm RMG and TS wafers. First of all, RMG W-gate conductance is tested on 15 repeating serpentine structures laid out across the die. These are 14 nm ground-rule test structures with the same pitch, dimension, and pattern density, but otherwise oriented differently (e.g., vertically vs. horizontally) and positioned randomly within a die. Two wafers each are polished with POR vs. MR pads, to the same gate height target as confirmed by scatterometry measurement. One each wafer, 1 center die and 1 edge die are tested for WIDNU based on gate conductance. The results are presented in Fig. 8. Due to different orientation and surrounding environment, some of the test structures, notably 2, 3, 9, 10, and 15 exhibit higher conductance than the others, suggesting underpolish. On the other hand, structures 4, 11, and 13 tend to show lower conductance, suggesting overpolish or dishing/erosion. Nevertheless, such within-die conductance variation is much less pronounced with MR pad than POR on both center and edge dies. The normalized range of conductance with respect to mean is ∼10% for MR pad, but >22% for POR.

Post RMG CMP wafers are subjected to bright-field defect scan with SEM inspection to determine the type of defects. A unique localized metal loss defects has been detected on specific devices and patterns. As shown in Fig. 9, MR pad results in less such defects on

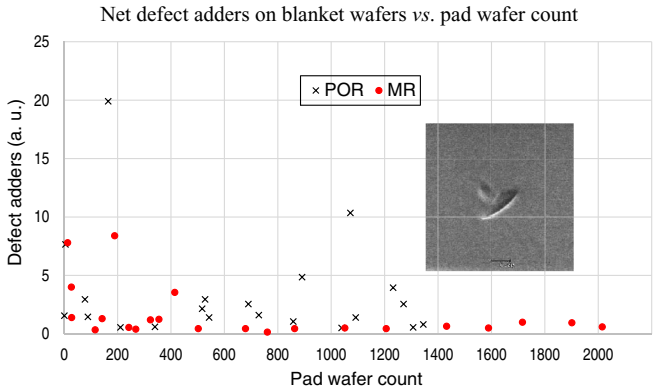

Figure 7. Net defect adders on blanket wafers vs. wafer count for POR and MR pads.

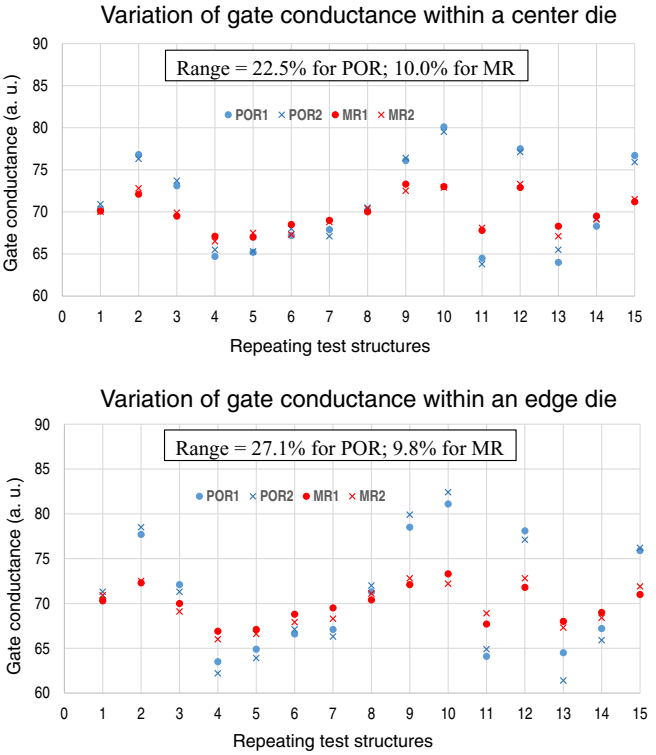

Figure 8. Within-die uniformity of wafers polished with POR vs. MR pads. Two wafers were polished and tested with each pad. Within each wafer, 15 repeating structures within a die with different orientation are tested for their gate electrical conductance on a center die and an edge die, and the range of conductance is normalized with respect to the mean.

these specific patterns than POR. It is hypothesized that, owing to the highly regulated surface features, MR pad is capable of polishing across varying pitches and pattern densities more uniformly without inducing excessive dishing and erosion to cause the metal loss. In other words, MR pad is less sensitive to pattern density effects. In fact, the superior conductance within-die uniformity in Fig. 8 is another indication of MR pad's lower pattern density dependence.

To verify the within-die uniformity from electrical tests, cross-sectional TEM samples are taken after RMG CMP to measure the total gate height on top of 3 different devices from dies at wafer center,

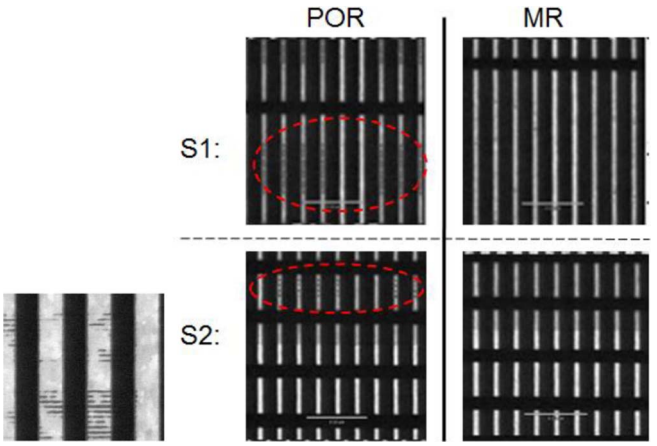

Figure 9. Localized metal loss detected post RMG CMP (highlighted on the left). Two structures, S1 and S2 are inspected for such defects. Circled areas on POR wafers show substantial metal loss while MR wafers are clear of such defects.

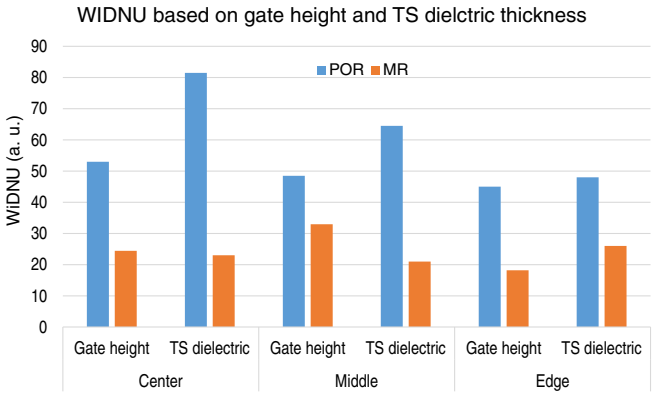

Figure 10. Within-die non-uniformity (WIDNU) determined by gate height range among 3 different devices, and by the range in dielectric thickness on top of gate (i.e., TS dielectric) between 3 different devices. One center die, one middle die, and one edge die from wafers polished with POR and MR pads are submitted for cross-sectional TEM analysis, from which gate height and dielectric thickness measurements are taken.

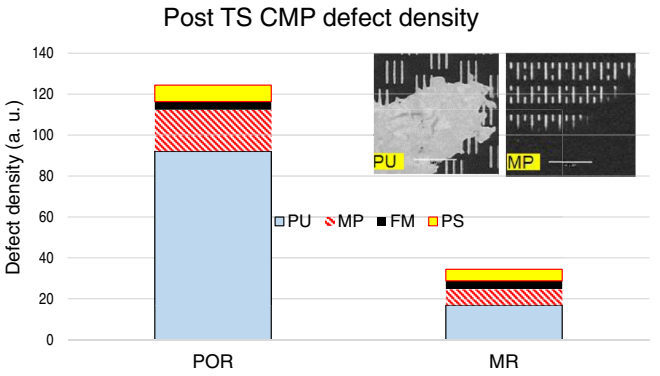

Figure 11. Post TS CMP defects between POR and MR pads. 3 wafers processed with each pad are inspected and their mean defect densities with classifications are presented. PU = puddle; MP = missing pattern; FM = foreign material; PS = polish scratch.

mid-range, and edge. On each die, WIDNU is defined as the gate height range of the 3 devices. A separate set of integrated wafers continue the process flow down to TS CMP with POR vs. MR pads. They are then submitted for cross-sectional TEM analysis to measure the TS dielectric, i.e., dielectric thickness directly on top of W-gate across the 3 same devices. Similarly, in this case, WIDNU is defined as the range of TS dielectric thickness across the 3 devices within the specific die. The resulting WIDNU based on the above *physical measurements* is summarized in Fig. 10. On all 3 dies, MR pad gives rise to less variation in both RMG gate height and TS dielectric thickness among the 3 devices than POR.

The application of MR pad to P3 buff of RMG CMP not only reduces variation in dishing and erosion due to pattern density effects, but can also help mitigate the thickness and local topography variation incoming to the down-stream TS module. Another consequence of such planarity improvement in RMG by MR pad is the reduction of topography-driven defects revealed after TS CMP. Figure 11 summarizes the post TS CMP defect density between POR and MR pads. 3 wafers from each pad are inspected after CMP. The wafers processed with MR pad for TS CMP were also processed with MR pad for RMG CMP before, likewise for POR wafers. Two major types of prior-level topography driven defects, puddle (PU) and missing pattern (MP) are detected. Puddle represents a "pool" of residual W difficult to remove due to recess/dishing from prior level (e.g., RMG). To a lesser degree, such pre-existing prior-level local topography variation can interfere with lithography depth-of-focus, causing missing pattern (MP) defects at the current level. Similarly, the existence of foreign material (FM), polish residue (PR), and polish scratches (PS) at prior level can all lead to MP defects too. As anticipated, wafers processed with MR pad for RMG and TS CMP show much less PU and MP defects. Meanwhile, *at-level* CMP-related defects such as FM and PS are about equivalent between POR and MR pads post TS CMP.

Post marathon pad analysis.—The used MR pad from 2000 W marathon test is subjected to extensive post analysis, including remaining asperity height measurement, and SEM inspection to check for the dimensional integrity of grooves, unit cells, asperity, and pores from pad center to edge. As shown in Fig. 12, on average, asperity height is reduced by about 10 μm, with minimum remaining asperity of ~9 μm occurring between 7 to 10 inches from pad center. Compared with pre data, the amount of total pad wear is between 3 μm and 12 μm. For comparison, the total amount of pad wear on used POR pad after 1300 wafer run is between 150 μm and 250 μm as shown in Fig. 13. Obviously, without the use of diamond tip conditioner, the amount of pad wear is much less on the MR pad and is mainly the consequence of pad-abrasive-wafer 3-body contact, plus, to a much less degree, the friction between pad and the bristle brush cleaner.

Fig. 14 shows post SEM inspection on the used MR pad. Slight distortion on edge of grooves is observed. Otherwise the microreplicated unit cells of asperity and pores remain intact. In addition, no

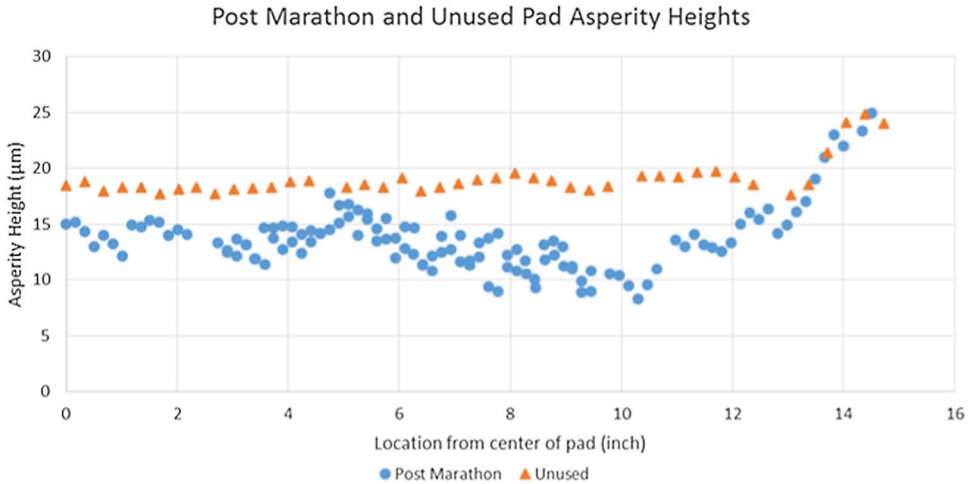

Figure 12. Asperity height profile of pre- and post 2000 W marathon MR pads. Total pad wear is between 3 μm and 12 μm.

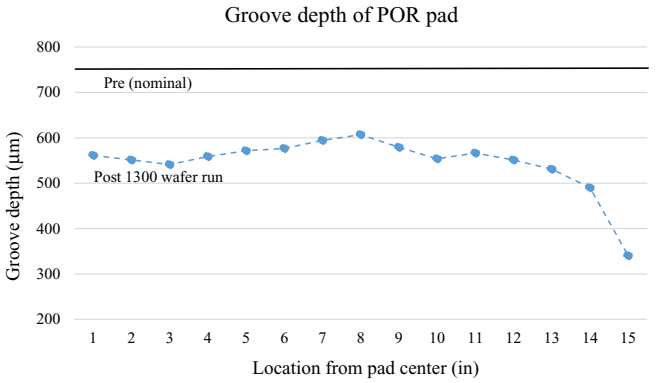

Figure 13. Groove depth profile of used POR pad post 1300 wafer run. Total pad wear is between 150 μm and 250 μm.

debris or residues are observed by SEM. The used pad surface appears very clean.

Evolution of CMP pad technology.—Polish pads with 3-dimensional microreplicated patterns on the surface represent a new milestone in the evolution of CMP technology. As illustrated in Fig. 15, the conventional CMP pads polish and planarize wafer surface features through 3-body asperity contact along pad/abrasive/wafer interface. The randomness in pad asperities and abrasive particle distribution introduces local variation in pressure and slurry flow inevitably, leading to WIWNU, WIDNU and sensitivity to pattern density effects. The introduction of fixed abrasive pads marks a leap forward toward CMP planarity improvement through pad technology. In this case, mounted abrasives with regulated spacing and fixed morphology provided enhanced planarization efficiency. When combined with high-selectivity abrasives (e.g., ceria), fixed abrasive pads demonstrated excellent planarization efficiency to reduce WIDNU. The application of microreplication technology to produce high-order regulated surface patterns *directly* onto the pad surface is another step forward to CMP planarity improvement. Conceptually similar to fixed-abrasive pads, MR pads with regulated spacing and fixed dimension provides uniform asperity contacts and enables uniform removal of "up" features. The dual or multiple asperity heights on MR pads provide secondary planarization capability. The significant reduction in WIDNU observed in the current study confirms the benefits of MR pad design. In addition, the high-order microreplicated patterns facilitate more efficient slurry delivery and debris transport, leading to potential for slurry saving and defect reduction. Last but not the least, the 3-dimensional microreplicated asperities obviate the need for conventional *pad dressing* with diamond tips conditioners. In fact, the 2000 wafer marathon test results in the current study provide the evidence that such MR pad can last at least as long as conventional pads with enhanced run-to-run, wafer-to-wafer repeatability.

The benefits demonstrated with MR pads open up numerous opportunities for further work in this new and evolving pad technology.

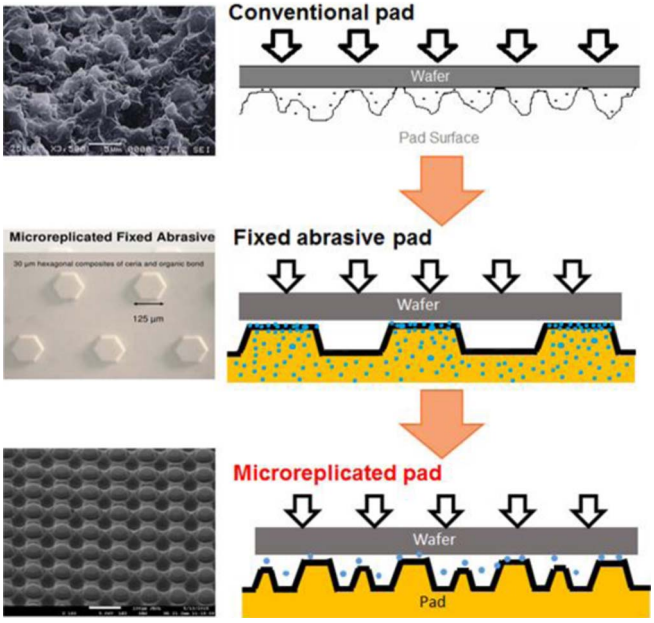

Figure 15. Evolution of CMP pad surface pattern.

Variables such as design and dimension of microreplicated patterns (asperity + pores), the lay-out of unit cells, and the width and depth of grooves, to name a few, can all interact in a way as to modulate the removal rates, uniformity, defectivity, and planarization efficiency. In addition, just like conventional pads, different MR pad designs and characteristics would be required to tailor for other applications, such as bulk oxide or Cu CMP, where, for example, the removal rates and planarity requirement are different.

Conclusions

A microreplicated CMP pad is applied to the buff step for 14 nm RMG and TS W-CMP and demonstrates the following benefits in a high-volume 300 mm wafer manufacturing environment:

- CMP process with more consistent wafer-to-wafer stability and repeatability in removal rates, WIWNU, and defectivity up to 2000 wafer passes than conventional pad with diamond tip conditioner.
- Significant reduction in WIDNU as confirmed by gate conductance electrical test and physical gate height and TS dielectric measurement by TEM.
- Reduction in *at-level* metal loss defects after RMG CMP, plus reduction in *prior-level* topography-driven defects such as puddle and missing pattern after TS CMP.

Post 2000 W marathon pad analysis reveals about 10 μm of asperity height reduction. The dimension and integrity of the microrepli-

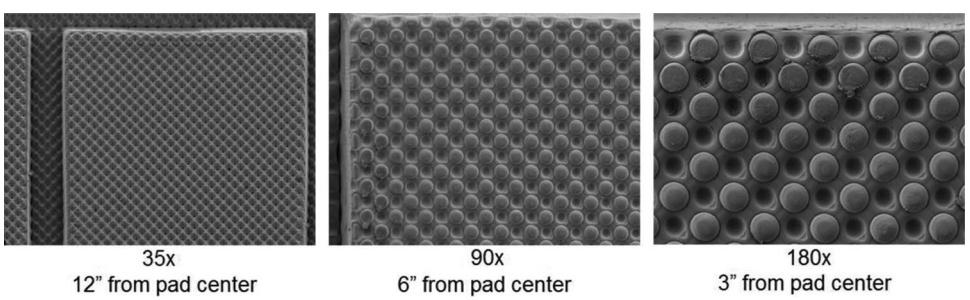

Figure 14. Post 2000 W marathon top-down SEM inspection of the used MR pad.

cated unit cells remain intact. The improvement in gate height and TS dielectric thin-die uniformity and defect reduction represent critical performance gain for advanced semiconductor devices with replacement metal gate integration. Varying microreplicated surface patterns tailored for different CMP applications should be the subject of future work of this new and evolving pad technology.

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